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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,610	12/05/2003	Jeffrey W. Sharp	017083.0286	2920

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EXAMINER	
DIAMOND, ALAN D	
ART UNIT	**PAPER NUMBER**
1753	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,610	SHARP, JEFFREY W.	
	Examiner	Art Unit	
	Alan Diamond	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004 and 03 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *03112005*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Comments

1. The objections to the drawings for informalities have been overcome by Applicant's amendment of the drawings and specification.

2. The objection to the specification for informalities has been overcome by Applicant's amendment thereof.

3. The objection to claim 3 for informalities has been overcome by Applicant's amendment thereof.

4. The Examiner acknowledges that claim 1 has been cancelled.

5. The indicated allowability of claim 3 is withdrawn in view of the newly discovered reference JP 10-242536 A (JP '536). Rejections based on the newly cited reference follow. On January 28, 2003, the Examiner had proposed (in order to place the case in condition for allowance), and applicant had agreed to amend claim 2 so as to recite that the P/N-type wafer is an extruded P/N-type wafer and that wherein common boundaries between the P-type regions and the N-type regions represent the compression and deformation experienced during the extrusion. However, upon reconsideration, such an amendment would not place the case in condition for allowance because JP '536's thermoelectric chip **A** is an extruded P/N-type wafer that would inherently have said common boundaries due to the extrusion (see Figures 1, 2, 8, and 9; and paragraphs 0036 to 0048, and 0054 to 0060).

6. On the page labeled No. 2 of the amendment to the specification filed November 24, 2004, at approximately midway through the page, applicant recites "Please amend

the paragraph that begins on page 10, line 25 ...". Please note that the paragraph begins on page 10, line 26, not line 25. The Examiner has changed the "25" to "26" on said page No. 2 of said amendment and initialed and dated the margin of said page No. 2. The corrected page No. 2 of said amendment will be scanned into the IFW file.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 2, 3, 5, and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 10-242536 A, herein referred to as JP '536.

JP '536 teaches a thermoelectric device comprising thermoelement chip, i.e. p/n-type wafer **A** comprising a plurality of p-type regions **1a** and a plurality of n-type regions **1b** interspersed between and adjacent the p-type regions; a patterned metallization **2** of copper or nickel coupled with the p-type and n-type regions; and first and second heat exchange plates **11** coupled with the p/n-type wafer **A** (see Figures 1(e), 1(f), 2(b), 8, and 9; and paragraphs 0033 and 0050).

With respect to claim 3, the p-type and n-type regions **1a, 1b** are connected in series by said metallization **2** (see paragraph 0033). Based on this series connection, and the heat exchange plates **11** at the top and the bottom, then said p-type and n-type regions **1a, 1b** are thermally in parallel.

With respect to claim 5, as seen in Figure 2(b), the number of p-type regions and n-type regions is equal.

With respect to claims 7 and 8, the p-type and n-type regions in the wafer **A** clearly have a "generally rectangular" cross-section, as seen in Figures 1(e), 2(b), 9(a). alternatively, the cross-section can be circular since the thermoelement ingredient **6** can be cylindrical instead of rectangular (see paragraph 0052).

With respect to claim 9, an insulating layer **13** (i.e., passivating agent) can be disposed upon a surface of the n-type and p-type regions (see paragraphs 0055 and 0059; and Figures 2(a) and 2(b)).

Since JP '536 teaches the limitations of the instant claims, the reference is deemed to be anticipatory.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 10-242536 A (herein referred to as JP '536) in view of Schlicklin et al (U.S. Patent 4,730,459).

JP '536 teaches a thermoelectric device comprising thermoelement chip, i.e. p/n-type wafer **A** comprising a plurality of p-type regions **1a** and a plurality of n-type regions **1b** interspersed between and adjacent the p-type regions; a patterned

metallization **2** of copper or nickel coupled with the p-type and n-type regions; and first and second heat exchange plates **11** coupled with the p/n-type wafer **A** (see Figures 1(e), 1(f), 2(b), 8, and 9; and paragraphs 0033 and 0050).

With respect to claim 3, the p-type and n-type regions **1a, 1b** are connected in series by said metallization **2** (see paragraph 0033). Based on this series connection, and the heat exchange plates **11** at the top and the bottom, then said p-type and n-type regions **1a, 1b** are thermally in parallel.

With respect to claim 5, as seen in Figure 2(b), the number of p-type regions and n-type regions is equal.

With respect to claims 7 and 8, the p-type and n-type regions in the wafer **A** clearly have a "generally rectangular" cross-section, as seen in Figures 1(e), 2(b), 9(a). alternatively, the cross-section can be circular since the thermoelement ingredient **6** can be cylindrical instead of rectangular (see paragraph 0052).

With respect to claim 9, an insulating layer **13** (i.e., passivating agent) can be disposed upon a surface of the n-type and p-type regions (see paragraphs 0055 and 0059; and Figures 2(a) and 2(b)).

JP '536 teaches the limitations of the instant claims other than the differences which are discussed below.

With respect to claims 4 and 6, JP '536 shows an equal number of n-type and p-type regions, but does not specifically teach more p-type regions than n-type regions or more n-type regions than p-type regions. Schlicklin et al teaches a thermoelectric module wherein there is an odd number of total p-type and n-type elements so that

there is either one more p-type element than the n-type elements, or there is one more n-type element than the p-type elements (see col. 2, lines 46-54; col. 4, lines 54-58). Doing this, as opposed to using an equal number of n-type and p-type elements, provides the advantage of thermal efficiency and electrical current at a relatively high voltage and a relatively low amperage (see col. 1, lines 28-59; and col. 2, lines 46-58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified JP '536's thermoelectric device so as to use an odd number of total n-type and p-type regions (i.e., one more p-type region than the n-type regions, or one more n-type region than the p-type regions) as opposed to and equal number of total n-type and p-type regions because said odd number of total p-type and n-type regions provides the advantage of thermal efficiency and electrical current at a relatively high voltage and a relatively low amperage, as taught by Schlicklin et al.

With respect to claim 11, JP '536 does not specifically teach a thermoelectric circuit having plural of its thermoelectric chips (i.e., instant individual legs) arranged electrically in series and thermally in parallel. Schlicklin et al shows the conventionality of a thermoelectric circuit having plural thermoelectric modules **M1**, **M2**, **M3** arranged electrically in series and thermally in parallel (see col. 7, line 59 through col. 8, line 22; and more particularly Figure 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have prepared a thermoelectric circuit using plural of JP '536's thermoelectric chips arranged electrically in series and thermally in parallel because such a thermoelectric circuit structure is conventional in the art, as shown by Schlicklin et al.

11. Claims 2, 3, 5, and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 10-242536 A (herein referred to as JP '536) in view of Mitchell et al (U.S. Patent 3,601,887).

JP '536 teaches a thermoelectric device comprising thermoelement chip, i.e. p/n-type wafer **A** comprising a plurality of p-type regions **1a** and a plurality of n-type regions **1b** interspersed between and adjacent the p-type regions; a patterned metallization **2** of copper or nickel coupled with the p-type and n-type regions; and first and second heat exchange plates **11** coupled with the p/n-type wafer **A** (see Figures 1(e), 1(f), 2(b), 8, and 9; and paragraphs 0033 and 0050).

With respect to claim 3, the p-type and n-type regions **1a, 1b** are connected in series by said metallization **2** (see paragraph 0033). Based on this series connection, and the heat exchange plates **11** at the top and the bottom, then said p-type and n-type regions **1a, 1b** are thermally in parallel.

With respect to claim 5, as seen in Figure 2(b), the number of p-type regions and n-type regions is equal.

With respect to claims 7 and 8, the p-type and n-type regions in the wafer **A** clearly have a "generally rectangular" cross-section, as seen in Figures 1(e), 2(b), 9(a). alternatively, the cross-section can be circular since the thermoelement ingredient **6** can be cylindrical instead of rectangular (see paragraph 0052).

With respect to claim 9, an insulating layer **13** (i.e., passivating agent) can be disposed upon a surface of the n-type and p-type regions (see paragraphs 0055 and

0059; and Figures 2(a) and 2(b)). This insulating layer **13** can be made from resin, glass, or ceramics, etc (see paragraph 0055).

JP '536 teaches the limitations of the instant claims other than the difference which is discussed below.

JP '536 does not specifically teach that said insulating layer **13** can be made from boron nitride (BN). Mitchell et al teaches that the insulating material between thermoelectric bodies can be an electrical insulator, such as BN, glass, etc (see col. 3, lines 5-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used BN for the electrical insulator **13** between JP '536's n-type and p-type thermoelectric regions because BN is a conventional electrical insulator to be used between thermoelectric bodies in a thermoelectric device, as shown by Mitchell et al.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. JP 10-56210 A is hereby made of record.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan Diamond whose telephone number is 571-272-1338. The examiner can normally be reached on Monday through Friday, 5:30 a.m. to 2:00 p.m. ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alan Diamond
Primary Examiner
Art Unit 1753

Alan Diamond
March 14, 2005
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